Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 40898

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018
Second Semester
Computer Science and Engineering
CS6201 – DIGITAL PRINCIPLES AND SYSTEM DESIGN
(Common to : Information Technology)
(Regulations 2013)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Why NAND and NOR gates are called Universal gates ?
2. Convert the following number from one base to another : $(76.4)_8 = (?)_{10}$.
3. State the different modeling techniques used in HDL.
4. Draw the truth table of Full adder.
5. What is the drawback of SR flip-flop ? How it is avoided in JK flip-flop ?
6. List the different types of shift registers.
7. What are the different techniques used in state assignment ?
8. Define Hazard.
9. How many address lines and data lines are there in 4K X 8 ROM ?
10. How many check bits are required for single bit error detection and correction ?

PART – B (5×16=80 Marks)

11. a) Simplify the following function using Karnaugh map method :

$F(A, B, C, D) = \Sigma m(0, 2, 5, 8, 10, 15) + \Sigma d(4, 14)$

and implement the circuit using only NOR gates.

(OR)

b) Simplify the following Boolean Expression using Tabulation method and construct the logical circuit using only NAND gates.

$F(A, B, C, D) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$.

12. a) With suitable illustration explain the operation of BCD adder. (16)

(OR)

b) Design 5 to 32 decoder using combination of 2 to 4 and 3 to 8 decoders. (16)

13. a) Design Synchronous Mod 10 counter using D flip flop. (16)

(OR)

b) Write the structural VHDL description of Universal 4 bit shift register. (16)

14. a) Design an asynchronous sequential circuit that has two inputs X_1 and X_2 and one output Z. When $X_1 = 0$, the output $Z = 0$. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0. (16)

(OR)

b) Write a detailed note on Hazards. (16)

15. a) i) Design and implement 3 bit binary to Gray code converter using PLA. (8)

ii) The Hamming code 101101101 is received. Correct it if any errors. There are four parity bits and odd parity is used. (8)

(OR)

b) Write a detailed note on sequential programmable devices. (16)

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